# WIDEBAND ENHANCED DIGITAL INJECTION PREDISTORTION FOR HIGH EFFICIENCY TRANSMITTERS

## FIELD OF THE INVENTION

The present invention is directed to linearization of high efficiency, high power RF amplifiers and related systems and methods.

## BACKGROUND, PRIOR ART AND RELATED INFORMATION

Modern wireless communication systems employ spectrally efficient, digitally modulated signals with wide bandwidths and time-varying envelopes. Variations in the envelope magnitude of digital modulations generate distortion components at the output of the transmitter that are caused by the inherent nonlinearity of RF amplification circuits. Amplifier distortion produces a dilation of the spectrum of the input signal ("spectral regrowth") which causes interference to communications in adjacent channels. Adjacent channel interference (ACI) is a highly undesirable phenomenon that is tightly controlled by regulatory organizations (FCC, ETSI, ITU). In addition to spectral regrowth, amplifier nonlinearities produce in-band distortion (i.e. distortion components within the bandwidth of the modulated input signal) which deteriorates the integrity of the transmitted signal and results in high BER at the receiver end. Nonlinearities in conventional RF amplifiers (Class AB) are relatively minor (distortion ~= 40 dB below the level of the carrier for output backoffs (OBO) = peak-to-average power ratio (PAR) of the modulation). The price to pay for such a mild nonlinear behavior is poor efficiency, i.e. limited DC-to-RF power conversion performance. High efficiency amplification is highly desirable since it improves system reliability (longer MTBF), simplifies thermal management, reduces amplifier size (lower silicon requirements) and lowers the operational and ownership costs of base stations. High efficiency amplifiers (e.g. Doherty) on the other hand exhibit much

more nonlinear behavior than Class AB designs (distortion <= 29 dB below the level of the carrier). One simple method of linearization increases the level of OBO in order to reduce output distortion by extending the linear range of operation of the amplifier. This technique can be successfully applied to enhance the linearity of Class AB amplifiers. Unfortunately it also produces a severe loss in efficiency due to reductions in RF output power resulting from higher OBO levels. High efficiency amplifiers on the other hand cannot typically be linearized by simply increasing OBO and require more sophisticated linearization techniques. A well-established technique uses Cartesian (or polar) feedback systems to minimize the output distortion of the amplifier. Feedback linearization can be effective for narrow signal bandwidths but has very limited distortion correction capabilities when wide bandwidth operation is required (e.g. multicarrier WCDMA) due to input-output stability restrictions associated to loop dynamics. Feedback would not be sufficient to linearize wide bandwidth, highly efficient transmitters. Another technique, feed forward, is based on additive post-correction of amplifier distortion, typically employing a dual loop architecture to estimate the output distortion of the amplifier in a first (carrier cancellation) loop and then injecting said distortion estimate, properly phased and scaled, to the output of the ("main") amplifier via an RF auxiliary or "error" amplifier (distortion cancellation loop). Feed forward linearization systems do not suffer from the bandwidth limitations of feedback linearizers and are unconditionally stable. However, and despite having wide bandwidth distortion correction capabilities, feed forward systems usually have low efficiency due to the DC power consumption of the error amplifier and the presence of lossy delay elements at the output of the main amplifier required for phase alignment of the distortion cancellation loop. Luckily there exists an alternative technique suitable for high linearity and high efficiency amplification: predistortion linearization. Conceptually and as a first order approximation, the predistortion technique linearizes the amplifier by injecting a compensatory distortion component at the input of the amplifier whose phase is opposite (180 degrees out of phase) to that of the

amplifier's output distortion and whose amplitude is that of the output distortion divided by the linear gain of the amplifier. Predistortion does not suffer from the stability and severe bandwidth restrictions of feedback linearization systems. It also has the advantage (over back-off and feed forward linearization) that its application in a well-designed system does not result in a severe degradation of amplifier efficiency. Due to these inherent advantages, predistortion linearization has been the subject of intense research over the past decade.

The prior art has mostly focused on the design and implementation of digital LUT (Look Up Table) predistorters given the flexibility, precision and noise immunity advantages that they typically offer in comparison to analog predistorters. In these LUT based systems predistortion is carried out in baseband in either polar or Cartesian coordinates. In polar digital predistortion systems a conversion between Cartesian/polar coordinates is usually necessary due to the fact that the digital input modulation is in quadrature form. The coefficients of the predistorter are adaptively computed and stored in tables indexed by transformations of the input (or output) signal envelopes. A number of prior art LUT predistorters are intended to only compensate for nonlinear static amplifier distortion, without provisions for the linearization of dynamic nonlinearities in the amplifier. These "static" predistorters are not well suited for high efficiency base station transmitter designs due to the fact that nonlinear dynamic distortion components or "memory effects" constitute a substantial portion of the total output distortion of high power, high efficiency amplifiers. Aware of this fact, some predistortion designers have conceived nonparametric digital baseband predistorters in which multidimensional tables are indexed by dynamic transformations (filtered versions) of the instantaneous input envelope magnitude or power. The main advantage of the multitable technique for nonlinear dynamic distortion compensation is that it does not require the computation of a parametric model of the inverse dynamics of the amplifier. The main disadvantages are large memory requirements for storing the predistortion coefficients and the computational

complexity involved in the interpolation of table entries when there is unreliable/insufficient data for system adaptation. Multitable interpolation complexity can be quite substantial, posing a limit to the accuracy and adaptation rate of the predistorter. The accuracy of digital LUT predistorters is also limited by table quantization errors. Quantization errors can severely limit distortion correction in high efficiency, high power transmitters in which wideband dynamic distortion compensation is necessary to meet stringent emissions specifications. A simple way to minimize table quantization error would be to increase table size. This solution is a viable alternative for some applications employing parametric digital LUT predistorters. Unfortunately increasing the number of table entries in multitable designs is prohibitive due to the rapid increase in memory and computational requirements. To improve the accuracy and lower the complexity of LUT predistorters a number of other predistortion systems have been proposed. However, none of these approaches adequately addresses the above problems.

The present invention is directed to overcoming the above noted shortcomings of the prior art and providing a predistortion system suitable for wide bandwidth applications without introducing undue complexity into the system.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 shows a functional block diagram of a predistortion linearized amplifier using an additive predistortion architecture in accordance with a preferred embodiment of the present invention.

FIGURE 2 shows a functional block diagram of a predistortion linearized amplifier using a multiplicative predistortion architecture in accordance with an alternate embodiment of the present invention.

FIGURE 3 shows a block diagram of the polynomial predistorter in accordance with a preferred embodiment of the present invention.

FIGURE 4 shows a block diagram of a predistortion linearized amplifier system that employs an additive predistortion architecture in accordance with a preferred embodiment of the present invention.

FIGURE 5 shows a block diagram of a predistortion linearized amplifier system that employs a multiplicative predistortion architecture in accordance with a preferred embodiment of the present invention.

FIGURE 6 shows a flow chart diagram of a predistortion adaptation algorithm in accordance with a preferred embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a new digital baseband predistorter with enhanced distortion correction capabilities. The predistorter uses a polynomial formulation to accurately predistort the amplifier. Accurate predistortion is achieved by providing separate and simultaneous compensation for nonlinear static, nonlinear dynamic and linear dynamic in-band distortion (including analog quadrature modulation errors) as depicted in the functional diagram of FIGURE 1. Compensatory predistortion components emerging from the linear dynamic, nonlinear dynamic and nonlinear static branches of the predistorter are summed together to form a unique distortion compensation signal. FIGURE 1 shows an additive predistorter and predistortion linearized amplifier in accordance with the present invention in which the distortion compensation signal is added (injected) digitally to the baseband modulation input to form the predistorted signal to drive the amplifier. FIGURE 2 shows a multiplicative predistortion arrangement in which the digital polynomial predistorter acts as a nonlinear operator in cascade with the amplifier.

The block diagram in FIGURE 3 shows the structure of the digital polynomial predistorter (DPPD) in accordance with a preferred embodiment of this invention. The baseband input to the DPPD (input modulation) in quadrature (I,Q) format is digitally filtered by a linear dynamics compensation block whose output is added to the nonlinear distortion compensation signal components generated by the predistorter. These components are generated by performing nonlinear transformations of the magnitude envelope of the DPPD input, computed using a digital envelope detector. The output of the digital envelope detector is filtered using a finite impulse response (FIR) filter to generate a distortion compensation signal in response to variations in envelope magnitude dynamics. Higher order dynamic distortion compensation components are generated by computing different powers of the envelope magnitude with signal multipliers and filtering

the multiplier's outputs using FIR filters. This arrangement provides selective compensation for reactive memory effects of different orders which are associated to the video bandwidth of the bias network and the electrical dynamics of the amplifier. Reactive memory effects constitute a significant portion of the total output distortion of the amplifier and must be compensated for to ensure acceptable linearity and efficiency performance. Note that FIGURE 3 depicts a predistorter that provides $7^{th}$ order reactive memory effect compensation only. Higher order compensation can be readily implemented by adding additional reactive memory compensation branches. Nonlinear static distortion compensation is computed by performing a static polynomial transformation of the output of the digital envelope detector. The outputs of the reactive memory compensation elements and the nonlinear static compensation block are summed together and used to drive an autoregressive dynamics compensation block implemented using an all-pole infinite impulse response (IIR) digital filter. The autoregressive dynamics compensation block cancels the distortion due to thermal drifts and long-term dynamics in the amplifier. The output of the autoregressive dynamics compensation block is used to modulate the I,Q baseband input to the DPPD. This modulated signal is added to the output of the linear dynamics compensation block to form the DPPD output.

FIGURE 4 shows a block diagram of a predistortion linearized amplifier system that employs an additive predistortion architecture, in accordance with the invention. The baseband input to the DPPD (input modulation) in quadrature (I,Q) format is predistorted by the DPPD and its output is added to the input modulation to form a digital baseband predistorted signal in cartesian coordinates. The in-phase and quadrature components of the digital baseband predistorted signal are converted into analog waveforms using digital-to-analog converters (DACs) and quadrature modulated to RF using an analog quadrature modulator (AQM). The predistorted carrier at the output of the AQM is used to drive the amplifier. A digital predistortion controller periodically compares the

digital baseband input modulation to an estimate of the complex baseband output envelope of the amplifier to adaptively modify the values of the DPPD parameters in order to ensure optimum linearity performance when changes in the operating conditions of the amplifier occur (thermal drifts, power supply fluctuations, changes in input modulation, variations in drive level, etc). The estimate of the complex baseband output envelope of the amplifier is obtained by RF sampling of the amplifier output using a directional coupler, RF to baseband frequency translation of the output signal employing a quadrature demodulator (AQDM) and digitatization of the quadrature demodulated complex envelope using analog-to-digital converters (ADCs). The up and down conversion processing of analog signals in the system are phase synchronized using a common local oscillator (LO) circuit. The DPPD controller can perform spectral analyses of the output envelope estimate to optimize the linearity of the amplifier in different frequency sub-bands.

FIGURE 5 shows a block diagram of a predistortion system that employs a multiplicative predistortion architecture, in accordance with the invention. The operation of the system is analogous to that described in FIGURE 4, the main difference being that the predistorter's topology in FIGURE 5 is multiplicative rather than additive as in FIGURE 4.

FIGURE 6 shows a flow chart diagram of the predistortion adaptation algorithm used in the invention and implemented in the DPPD controller. Estimates of the input signal to the amplifier (PA Input) are generated by a predictive DPPD filter inside the DPPD controller. The generated PA Input and the estimate of the complex baseband output envelope of the amplifier (PA Output) are processed by the Data Grabber block which selects N samples from PA Input and PA Output to form the data buffers to be used for DPPD adaptation. The data verifier then determines whether the samples selected by the data grabber are suitable for the computation of new predistortion parameters. If the data is good

then it is presented to the data synchronizer which uses fractional delay interpolation techniques to time-align the input and output data in order to compensate for amplifier and processing delays. Proper time synchronization is an important requirement for ensuring the accuracy of memory effect compensation in the DPPD. The time-aligned input and output data buffers are then processed by the Predistortion Model Builder which uses the synchronized data to compute a kernel matrix using the DPPD structure shown in FIGURE 3. The parameter calculator uses the kernel matrix and the synchronized input data to compute the predistorter's parameters. It uses fast convergence least square techniques to find an "optimal" set of parameter values that minimize the quadratic norm squared (average power) of the output distortion of the amplifier. The DPPD parameters are low-pass filtered in the parameter averager to reduce the effects of noise and disturbances in the computation of the DPPD parameters. Finally the predistortion model validator checks the consistency and validity of the parameter values computed by the parameter estimator and averaged by the parameter averager. The predistortion model validator keeps a table of previously computed predistortion coefficients that can be used in case that the most recently computed parameters estimates do not provide acceptable predistortion performance.

To summarize, the present invention provides the following features and aspects:

1. An additive digital baseband predistorter for high efficiency, highly nonlinear amplifiers:
    a. Employing a discrete-time polynomial kernel.
    b. Capable of separate and simultaneous compensation of linear dynamic, nonlinear dynamic and nonlinear static amplifier distortions.
    c. With embedded parametric thermal dynamics correction.
    d. Capable of frequency-selective monitoring of amplifier distortion.

e. Able to adaptively change the value of the polynomial predistorter's parameters in response to changes in the operating conditions of the amplifier.

2. A multiplicative digital baseband predistorter for high efficiency, highly nonlinear amplifiers:
   a. Employing a discrete-time polynomial kernel.
   b. Capable of separate and simultaneous compensation of linear dynamic, nonlinear dynamic and nonlinear static amplifier distortions.
   c. With embedded parametric thermal dynamics correction.
   d. Capable of frequency-selective monitoring of amplifier distortion.
   e. Able to adaptively change the value of the polynomial predistorter's parameters in response to changes in the operating conditions of the amplifier.